REMARKS

As a preliminary matter, Applicants appreciate the acknowledgement of allowable subject matter contained in claims 6-7, 13-14 and 23.

Claims 1-5, 8-12 and 15-22 stand rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (U.S. Patent No. 5,881,037). Applicants traverse the rejection because the cited reference does not disclose (or suggest) inserting a predetermined specific code train into the beginning head portion and ending last portion of data, as featured in the independent claims. Applicants further traverse the rejection because the cited reference does not disclose (or suggest) the feature of the present invention of eliminating the RLL code for clock extraction by inserting revise bytes ("predetermined specific code trains") (see, e.g., claim 2).

The Examiner cites Tanaka as teaching inserting a predetermined specific code train into at least two or more portions including head and last portions of data. However, Tanaka teaches dividing data blocks into plural sectors of plural frames. A "type information code" identifying the frame containing the sector address information is contained in the synchronization code inserted before the frame containing the sector address information (Col. 4, lns. 38-44).

In contrast, the present invention features storing revise bytes in the last portion of data. As illustrated in FIG. 6, revise bytes 50-n occur at the end of data 54-m. Accordingly, for at least this reason, claims 1, 8, 15 and 18 are believed to be allowable.

In addition, the present invention eliminates the RLL code for clock extraction, and in replacement thereof, inserts revise bytes that include a specific code train into data to record the data on the medium. Since the revise bytes consist of known data, a mistake in a determination value is avoided. Moreover, even when a reproduction signal has a low S/N ratio, stable clock extraction and

amplitude correction can be performed and the decoding performance or error rate can be improved. That is, because there is no RLL decoder, it is possible to eliminate error propagation caused by RLL decoding, and permit maximum use of the ECC correcting ability.

In contrast, with respect to RLL code, Tanaka discloses that data is decoded into an RLL code during recording. The RLL code is encoded into data upon reproducing. More specifically, as illustrated in FIG. 8, there is a coding unit 804 on the recording side in which the data is 8/15 converted in accordance with a conversion tail as shown in FIGs. 2 and 3. As further illustrated in FIG. 11, a decoder 1104 is provided on the reproducing side, and the 8/15 code that is reproduced is encoded to restore a code into the original data. Accordingly, Tanaka does not disclose or suggest the feature of eliminating the RLL code as featured in the claims of the present invention, for example claims 2, 9, 19 and new claim 24. That is, Tanaka does not teach eliminating the RLL code and replacing the code by inserting revise bytes as a specific code train into the data to record the data/revise bytes on the medium. Accordingly, dependent claims 2, 9, 19 and 24 should be allowed for these additional reasons. The remaining claims are considered allowable for the reasons stated above and based on their chain of dependency from independent claims 1, 8, 15 and 18, respectfully.

For all of the foregoing reasons, Applicants submit that this Application is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 
Joseph P. Fox
Registration No. 41,760

February 20, 2004

300 South Wacker Drive - Suite 2500
Chicago, Illinois 60606
Telephone: (312) 360-0080
Facsimile: (312) 360-9315
Customer Number 24978